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1. INTRODUCTION

The DAQP series PC card (including DAQP-12, DAQP-16, DAQPi-12, DAQPi-16, DAQP-12OM and DAQP-16 OM) is a PCMCIA type II data acquisition system with 8 differential or 16 single-ended analog input channels. The number of input channels can be expanded to 256 with input expansion cards. Each channel has a bipolar input range from ±1.25 V (gain = 8), ±2.5 V (gain = 4), ±5 V (gain = 2) to ± 10V (gain = 1) with programmable gains of 1, 2, 4 and 8. The DAQP series PC card supports sampling rates up to 100 kHz at either 12-bit or 16-bit resolution.

Equipped with a data FIFO of 512 (standard) or 2048 (those with the 2K option) samples, the DAQP series PC card can achieve full speed data acquisition under various operating platforms, including Microsoft DOS, Windows 3.xx and Windows 95. It also has a scan FIFO of the same size that supports full speed, random order channel scanning and gain selection for all the input channels (up to 256 channels when using the input expansion cards).

The DAQP series PC card has a 24-bit pacer clock and a programmable divided-by-2, by-10, or by-100 pre-scaler. The pacer clock can also be used with an external clock source. With the 10 MHz internal clock source, the pacer clock can generate accurate sampling rate from 0.006 Hz to 100 kHz.

The DAQP series PC card also has 4 digital input and 4 digital output channels, all of them TTL compatible, which may be used for control or monitoring in addition to analog data acquisition.

The software drivers provides supports for various programming languages like Microsoft C/C++, Borland C/C++, Delphi, QuickBasic, Visual Basic for DOS and Turbo Pascal. A Dynamic Link Library (DLL) is provided for all kinds of programming languages under Microsoft Windows, as well as the Visual Basic Controls (VBX). The DAQP series PC card also has turn-key software supports for LabTech NoteBook, Snap Master, LabView, TestPoint, and etc.

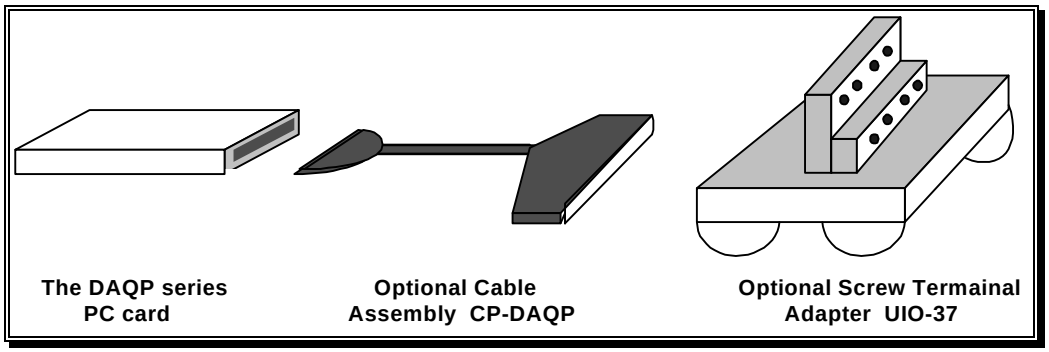

Figure 1. DAQP series PC card cable connection illustration

Figure 1 illustrates the DAQP series PC card cable connection. For users who do not want to interface to the PC card's 0.8 mm 33-pin I/O connector, an optional adapter cable is available to convert this connector into an industry standard D-37 male connector (female connector is also available). For applications requiring discrete wire hook-ups, an optional screw terminal adapter is also available to convert the D-37 connector into 37 discrete screw terminal blocks. These optional accessories are described in detail in chapter 9.

The DAQP series PC card offers the following features:

- 12 or 16 bit resolution
- 8 differential or 16 single-ended analog input channels, expandable to 256 channels
- Bipolar input range up to ±10 volts
- Truly programmable gain of 1, 2, 4, or 8
- Full speed channel scanning and gain selection for all analog input channels
- Data FIFO of 512 (standard) or 2048 (with the 2K option) samples
- Sampling rate up to 100 kHz
- 24-bit pacer clock with variable pre-scalers and external clock source
- Digital input/output channels
- Flexible trigger mode (internal/external, one-shot/continuous, rising/falling edge)
- Software drivers for DOS, Windows 3.xx, Windows 95, as well as canned software packages like LabTech NoteBook, Snap Master, LabView, and TestPoint.

2. INSTALLATION

2.1 HARDWARE SETUP

To install a DAQP series PC card, simply insert the adapter into any type II PCMCIA socket. All other configuration options are determined by the operating system, the Client Driver or the Enabler software as discussed in the following sections.

2.2 SOFTWARE SETUP WITH WINDOWS 95

An "INF" file has been provided in the customer software diskette for easy installation of the DAQP series PC card under Microsoft Windows 95. The operating system uses the "INF" file to determine what system resources are required by the board, searches for available resources to fill the boards requirements, configures the PC Card hardware, and then updates the hardware registry with an entry that allocates these resources.

2.2.1 Installing the DAQP Series PC Card

1. Insert the PC card in any available PCMCIA socket.
2. The first time a new PCMCIA card type is installed the "New Hardware Found" window opens. After this first installation Windows 95 automatically detects and configures the card. If the "New Hardware Found" window does not open, then skip to the next section, "Viewing the PCMCIA Card Settings".
3. The "New Hardware Found" window provides several options to configure the new PCMCIA card. Click the Driver from disk provided by hardware manufacturer option button. Click OK to continue.
4. An "Install From Disk" dialog box should pop up. Insert the customer diskette with the Windows 95 INF files on it, select the correct drive letter, and click the OK button. Windows 95 automatically browses the root directory for an INF file that defines configurations for the new hardware type found. If no INF files are found, click the Browse button and search the Win95 sub-directory on the installation diskette. You are not required to select the file name. After finding the directory containing the INF files, Windows 95 will choose the correct file.
5. Your new PCMCIA card should now be configured. In the future Windows 95 will automatically recognize and configure this PCMCIA card type.

2.2.2 Viewing the DAQP Series PC Card Status

1. Double click the "My Computer" icon located on the Windows 95 desktop. This opens a folder showing the various drives, printers, etc.
2. Double click the "Control Panel" icon. This opens another folder with many different system configuration utilities.
3. Double click the "PC Card (PCMCIA)" icon. This opens the "PC Card (PCMCIA) Properties" window.
4. The "PC Card (PCMCIA) Properties" window shows the status of your computers PCMCIA sockets. The DAQP series PC card should be listed in one of these sockets.
5. For changing the PC card configuration, see next section "Changing the Configuration of the PC Card".

Your hardware should now be properly installed and configured.

IMPORTANT:

If you are using Windows 95, section 2.3, chapter 3 and chapter 4 should all be ignored. The Windows 95 operating system takes care of the DAQP series PC card configuration completely. It is NOT allowed to use the DAQP series Client Driver or Enabler to configure any PC card under Windows 95.

2.2.3 Changing the Configuration of the PC Card

1. Double click the "My Computer" icon located on the Windows 95 desktop. Inside the "My Computer" folder, double click the "Control Panel" icon. This can also be done by clicking "Start", "Settings" and then "Control Panel".
2. Inside the "Control Panel" folder, double click the "System" icon so that the "System Properties" window pops up. Select the "Device Manager" stub. Find the "Data Acquisition" entry (preceded by the manufacturer's name or the vendor's name) from the device list. Expand the entry by clicking the leading "+" sign or by double clicking the name.
3. From the expanded sub-list, choose the PC card whose configuration needs changing (there may be only one entry) by double clicking it.
4. Select the "Resources" stub from the pop-up window. Highlight the resource type (either "Input/Output range" or "Interrupt Request") from the "Resource Setting" table (by clicking on it), and then click the "Change Settings ..." button. This pops up the "Edit Input/Output Range" or " Edit Interrupt Request" window.

5. Change the value by clicking on the slider controls by the "value" list and then click OK to confirm the change, or CANCEL to discard it. Watch for possible conflicts shown in the "Conflict Information" box.

The only configuration parameters that can be changed for the DAQP series PC card under Windows 95 are the "Input/Output Ranges" and the "Interrupt Request". They are, if required, the only ones that need to be changed, too.

2.2.4 Dealing with Difference in CIS

The DAQP series PC cards come with 12-bit and 16-bit versions, as well as standard (512 bytes) and 2K FIFO size options. Each version may also have different product names and product descriptions depending on the vendor or manufacturer names associated with the PC card. All this, except for the FIFO size options, results in differences in the CIS (Card Information Structure) of the PC card.

Even for the same DAQP series PC card there might have been changes in its CIS for various reasons (e.g., new fields added in for more accurate description of the card). Therefore, you might have the same product (so far as the hardware is concerned) in the series that has a different CIS.

The way the DAQP series PC cards are configured under Windows 95 is actually the same regardless of the differences in CIS, resolution (12-bit or 16-bit), FIFO size (with or without 2K FIFO size option), product name, product description, and vendor or manufacturer names.

However, Windows 95 will take it as a different PC card if it sees any difference in the CIS. We suggest that the INF file on the custom diskette that comes with the PC card be used. You need to install the INF file ONLY if Windows 95 does NOT recognize the DAQP series PC card when it is inserted into the system. If that is the case, follow steps described in section 2.2.1 to have it installed.

It is NOT necessary to install the INF file that comes with your new DAQP series PC card if it can be recognized by Windows 95 because an older version of the INF file has been installed in your system.

It is possible that there are more than one version of the INF files in the system. Windows 95 will automatically use the right one for its associated DAQP series PC cards. Once the association is established (e.g., through installation steps), Windows 95 will recognize it every time the PC card is inserted.

Unless absolutely necessary, do NOT try to modify, merge, rename, or delete the INF files in the system. Please report the problems, if any, to the technical support of your vendor or manufacturer. The phone numbers are usually listed on the title page of this manual.

2.3 SOFTWARE SETUP UNDER WINDOWS 3.xx AND DOS

Two software configuration programs are provided with the DAQP series PC card: a Client Driver named DAQP_CL.SYS, and a card Enabler named DAQP_EN.EXE. Either one of these programs may be used to configure the PC card **but only one may be used at a time**. The table below highlights the differences between the Client Driver and the Enabler program. The installation and usage of each of these programs is detailed in chapter 3 and 4.

Table 1. Comparison Between Client Driver and Enabler

Client Driver	Enabler
DAQP_CL.SYS	DAQP_EN.EXE
Interfaces to PCMCIA Card and Socket Services software (PCMCIA host adapter independent)	Interfaces directly to Intel 82365SL and other PCIC compatible PCMCIA host adapters
Allows automatic configuration of DAQP series PC card upon insertion (Hot Swapping)	Does not support automatic configuration of DAQP series PC card upon insertion (Hot Swapping)
Requires PCMCIA Card and Socket Services software	Does not require PCMCIA Card and Socket Services software

On systems with Card and Socket Services installed, the Client Driver is the preferred method of installation. If you are unsure whether Card and Socket Services software is installed, install the DAQP series Client Driver as discussed in chapter 3. When loaded, the Client Driver will display an error message if Card and Socket Services software is not detected.

3. USING THE CLIENT DRIVER

For systems using DOS and configured with PCMCIA Card and Socket Services software, a Client Driver named “DAQP_CL.SYS” is provided to configure the DAQP series PC cards. PCMCIA Card and Socket Services software is not provided with the DAQP series PC cards. However, it should be available from your vendor.

> IMPORTANT:
>
> Some versions of Card and Socket Services dated before 1993 do not support general purpose I/O cards. If after careful installation of the Client Driver the DAQP series PC card still does not configure or operate properly, an updated version of Card and Socket Services may be required.

The following procedure is used to install the DAQP series Client Driver:

1. Copy the file DAQP_CL.SYS from the DAQP series PC card distribution diskette onto the system's hard drive.
2. Using an ASCII text editor, open the system's CONFIG.SYS file located in the root directory of the boot drive.
3. Locate the line in the CONFIG.SYS file where the Card and Socket Services software is installed.
4. **AFTER** the line installing the Card and Socket Services software, add the following line to the CONFIG.SYS file:

   DEVICE = *drive*:*path*\DAQP_CL.SYS *options*

   where *options* are the DAQP series Client Driver command line options discussed on the following pages.
5. Save the CONFIG.SYS file and exit the text editor.
6. Insert the DAQP series PC card into one of the system's PCMCIA slots. **NOTE:** *Since the DAQP series Client Driver supports "Hot Swapping", it is not necessary to have the PC card installed when booting the system. By inserting the PC card before booting, however, the Client Driver will report the card configuration during the boot process thereby verifying the changes made to the CONFIG.SYS.*

7. Reboot the system and note the message displayed when the DAQP series Client Driver is loaded. If the Client Driver reports an "invalid command line option", correct the entry in the CONFIG.SYS file and reboot the system again. If the Client Driver reports "Card and Socket Services not found", then the Card and Socket Services must be installed on the system or the DAQP series enabler program must be used to configure the adapter (see chapter 4). If the Client Driver reports the desired adapter configuration, the installation process is complete and the DAQP series PC card may be removed and / or inserted from the system as desired. On each insertion into the PCMCIA socket, the PC card will automatically be reconfigured to the specified settings.

3.1 CLIENT DRIVER COMMAND LINE OPTIONS

The DAQP series Client Driver accepts up to eight command line arguments from the user to determine the configuration of the DAQP series PC card. If any arguments are provided, the DAQP series Client Driver will attempt to configure any DAQP series PC cards with the options specified in the order they are entered on the command line. Each argument must be enclosed in parenthesis and must be separated from other arguments by a space in the command line. Inside an argument, a comma (no space) should be used to separate the parameters from each other if there are two or more parameters. Within each argument, any or all of the following parameters may be specified:

B*address* specifies the base I/O address of the DAQP series PC card in hexadecimal. *address* must be in the range 100H - 3F8H and must reside on an even 8-byte boundary (*address* must end in 0 or 8). If this option is omitted, a base address will be assigned by Card and Socket Services.

I*irq* specifies the interrupt level (IRQ) of the DAQP series PC card in hexadecimal. *irq* must be one of the following values: 3, 4, 5, 7, 9, 10, 11, 12, 14, 15, or 0 if no IRQ is desired. If this option is omitted, an interrupt level will be assigned by Card and Socket Services.

S*socket* specifies the PCMCIA socket number to configure. *socket* must be in the range 0 - 15. If this option is omitted, the configuration argument will be applied any available DAQP series PC card inserted in any sockets in the system.

3.2 CLIENT DRIVER INSTALLATION EXAMPLES

When using the DAQP series Client Driver, the user may specify a list of selections (in the form of command line arguments) for the configuration of the DAQP series PC cards. The Client Driver scans this list from left to right until it finds a selection that is currently available in the system. If none of the preferred selections is available, the Client Driver requests a configuration from Card and Socket Services.

Example 1:

```
DEVICE = C:\DAQDRIVE\DAQP_CL.SYS
```

In example 1, no command line arguments are specified. The Client Driver will configure the DAQP series PC card into ANY socket with a base address and an IRQ level assigned by Card and Socket Services.

Example 2:

```
DEVICE = C:\DAQDRIVE\DAQP_CL.SYS  (b300)
```

In this example, a single command line argument is provided. The Client Drive will attempt to configure a DAQP series PC card inserted into ANY socket with a base address of 300H, and an IRQ level assigned by Card and Socket Services. If the base address 300H is not available, the PC card will NOT be configured.

Example 3:

```
DEVICE = C:\DAQDRIVE\DAQP_CL.SYS  (s0,b300,i5)
```

Provided in example 3 is also a single command line argument. The client Driver will attempt to configure the DAQP series PC card inserted in socket 0 at base address 300H and IRQ level 5. If either address 300H or IRQ level 5 is unavailable, the PC card will NOT be configured. In addition, the Client Driver will NOT configure any DAQP series PC card inserted into any socket other than socket 0.

Example 4:

```
DEVICE = C:\DAQDRIVE\DAQP_CL.SYS (b300,i5) (i10) ( )
```

Three command line arguments are provided in this example. The Client Driver will first attempt to configure a DAQP series PC card inserted into any socket with a base address 300H and IRQ level 5. If either address 300H or IRQ level 5 is unavailable, the Client Driver will proceed to the second command line argument and attempt to configure the card with a base address assigned by the Card and Socket Services and IRQ level 10. If IRQ level 10 is also unavailable, the Client Driver will then go to the third command line argument and attempt to configure it with a base address and an IRQ level assigned by the Card and Socket Services.

Example 5:

DEVICE = C:\DAQDRIVE\DAQP_CL.SYS (b300,i5) ( ) (i10)

The difference between example 5 and example 4 is the order of the second and the third command line argument. The Client Driver will first attempt to configure a DAQP series PC card inserted into any socket with a base address 300H and IRQ level 5. If either address 300H or IRQ level 5 is unavailable, the Client Driver will proceed to the second command line argument and attempt to configure the card with a base address and an IRQ level assigned by the Card and Socket Services. Since the second command line argument includes all available address and IRQ resources, third command line argument will never be reached by the Client Driver. It is the user's responsibility to place the command line arguments in a logical order.

Example 6:

DEVICE = C:\DAQDRIVE\DAQP_CL.SYS (s0,b300,i5) (s1,b310,i10)

There are two command line arguments in example 6, which is desirable in systems where two or more DAQP series PC cards are to be installed. The Client Driver will attempt to configure such a PC card in socket 0 with base address 300H and IRQ 5. If there is a DAQP series PC card in socket 1, it will be configured with base address 310H and IRQ 10. This allows the user to force the PC card's address and IRQ settings to be socket specific, as might be required by software or cable connection. However, if the requested resources are not available, the PC cards will not be configured.

3.3 COMMON PROBLEMS

3.3.1 Generic Client Drivers

Many Card and Socket Services packages include a generic client driver (or SuperClient) which configures standard I/O devices. If one of these generic client drivers is installed, it may configure the DAQP series PC card and cause the DAQP series Client Driver to fail installation. If this is the case, try the following:

1. Modify the operation of the generic client driver so that the DAQP series PC card will not be configured by the generic client driver. Consult the Card and Socket Services documentation for availability and details of this feature.

2. Place the DAQP series Client Driver before the generic client driver in the CONFIG.SYS file.

3.3.2 Available Resources

One function of the Card and Socket Services software is to track which system resources (memory addresses, I/O addresses, IRQ levels, etc.) are available for assignment to inserted PC cards. Sometimes, however, the Card and Socket Services assumes or incorrectly determines that a particular resource is unavailable when it is actually available. Most Card and Socket Services generate a resource table in a file (typically in the form of an .INI file) which the user can modify to adjust the available system resources. Consult the Card and Socket Services documentation for the availability and details of this feature.

3.3.3 Multiple Configuration Attempts

Some Card and Socket Services have a setting which aborts the configuration process after a single configuration failure (such as a configuration request for an unavailable resource). The user should change this setting to allow for multiple configuration attempts. Consult the Card and Socket Services documentation for the availability and details of this feature.

3.3.4 Older Versions of Card and Socket Services

Some versions of Card and Socket Services dated before 1993 do not support general purpose I/O cards like the DAQP series PC cards. If after careful installation of the DAQP series Client Driver the DAQP series PC card still can not be configured or operated properly, an updated version of Card and Socket Services may be required. Card and Socket Services software should be available from your vendor.

3.4 WHERE TO GO FROM HERE

The DAQP series PC card is now configured and ready for use. Depending on the type of application software to be used, the user may wish to review one or more of the following:

1. Chapter 5 of this document provides a basic theory of operation of the adapter for users who wish to learn the technical details about the operation of the DAQP series PC card.
2. For users who want to program the adapter with direct I/O transfers to the PC card's register set, chapter 7 provides an address map and a detailed description of each I/O register.
3. Users who would like to write custom application software without programming the DAQP series PC card directly should consult the DAQDRIVE software reference manual. DAQDRIVE provides a library of data acquisition subroutines for various data acquisition adapters and is included free of charge with the DAQP series PC card.
4. For turn-key data acquisition software (i.e. LabTech NoteBook, SnapMaster, LabView and TestPoint) consult the documentation provided by the software manufacturer.

4. USING THE ENABLER

For systems that are not operating PCMCIA Card and Socket Services software, the DAQP series PC card includes an Enabler program to enable and configure the PC card. This Enabler, DAQP_EN.EXE, will operate on any DOS system using an Intel 82365SL or PCIC compatible PCMCIA host adapter including the Cirrus Logic CL-PD6710 / 6720, the VLSI VL82C146, and the Vadem VG-365 among others.

IMPORTANT:

In order to use the DAQP series Enabler for DOS, the system must NOT be configured with Card and Socket Services software. If a Card and Socket Services software is installed, the Enabler may interfere with its operation and the devices it controls. Therefore, use DAQP series Client Driver or Enabler exclusively.

The DAQP series Enabler does not support automatic configuration of adapters upon insertion, more commonly referred to as “Hot Swapping”. This means the adapter must be installed in one of the system's PCMCIA sockets before executing DAQP_EN.EXE. If more than one adapter is installed in a system, the Enabler must be executed separately for each adapter. Furthermore, DAQP_EN.EXE should be executed to release the resources used by the adapter before it is removed from the PCMCIA socket. Since PCMCIA adapters do not retain their configuration after removal, any adapter that is removed from the system must be reconfigured with the Enabler after re-inserting it into a PCMCIA socket.

IMPORTANT:

The Enabler requires a region of high DOS memory when configuring the DAQP series PC card. This region is 1000H (4096) bytes long and by default begins at address D0000H (it may be changed by the “W” option as will be described later). If a memory manager such EMM386, QEMM or 386MAX is installed on the system, this region of DOS memory must be excluded from the memory manager’s control (normally by using the “x” switch). Consult the documentation provided with the memory manager software for instructions on how to exclude this memory region.

4.1 ENABLER COMMAND LINE OPTIONS

To configure a DAQP series PC card in the system, the Enabler requires one command line argument from the user to determine the configuration of the PC card. This argument must be enclosed in parenthesis. Within the argument, a comma (no space) must be used to separate the parameters from each other if there are two or more parameters. The following parameters may be specified in the command line argument:

S*socket* specifies the PCMCIA socket number where the DAQP series PC card is inserted for configuration. *socket* must be in the range 0 - 15. This option is always required.

B*address* specifies the base I/O address of the PC card in hexadecimal. *address* must reside on an even 8-byte boundary (*address* must end in 0 or 8). This option is required if the "R" option is not used.

I*irq* specifies the interrupt level (IRQ) of the PC card in hexadecimal. *irq* must be one of the following values: 3, 4, 5, 7, 9, 10, 11, 12, 14, 15, or 0 if no IRQ is desired. This option is required if the "R" option is not used.

W*address* specifies the base address of the memory window required to configure the PC card. Set *address* = D0 for a memory window at D0000, *address* = D8 for a memory windows at D8000, etc. Valid settings for *address* are C8, CC, D0, D4, D8, and DC. If omitted, *address* = D0 is assumed.

R instructs the Enabler to release the resources previously allocated to the PC card. When this option is used, "B" and "I" options will be ignored. Therefore, do NOT use this option when configuring the PC card into the system.

4.2 ENABLER EXAMPLES

Example 1:

DAQP_EN.EXE

No command line argument is specified. The Enabler will report an error and display the proper usage of the Enabler.

Example 2:

DAQP_EN.EXE (s0,b300,i5)

In this example, the Enabler will configure the PC card in socket 0 with a base address 300H and IRQ level 5 using a configuration memory window at D0000H.

Example 3:

DAQP_EN.EXE (i10,b310,s1)

In example 3, the Enabler will configure the PC card in socket 1 with a base address at 310H and IRQ level 10 using a configuration memory window at D0000H. Note that the parameter order is not significant.

Example 4:

DAQP_EN.EXE (s0,b300,i5,wCC)

Here the Enabler will configure the PC card in socket 0 with a base address at 300H and IRQ level 5 using a configuration memory window at CC000H.

Example 5:

DAQP_EN.EXE (s0,r)

DAQP_EN.EXE (s0,r,b300,i5)

These two command line arguments are equivalent because of the “r” option. The Enabler will release the configuration used by the PC card in socket 0 using a configuration memory window at D0000H.

Example 6:

DAQP_EN.EXE (s0,r,wC8)

Here the Enabler will release the configuration used by the PC card in socket 1, using a configuration memory window at C8000H.

4.3 COMMON PROBLEMS

4.3.1 Memory Range Exclusion

The Enabler requires a region of high DOS memory when configuring a DAQP series PC card. This region is 1000H (4096) bytes long and by default begins at address D0000H (this default address can be changed by using the "W" option). If a memory manager such as EMM386, QEMM or 386MAX is installed on the system, this region of DOS memory must be excluded from the memory manager's control (normally by using the "x" switch). Consult the documentation provided with the memory manager software for instructions on how to exclude this memory region.

Furthermore, some systems use the high memory area for ROM shadowing to improve overall system performance. In order for the Enabler to operate, any ROM shadowing must be disabled in the address range specified for the configuration window. This can usually be realized by using the system's CMOS setup utility.

4.3.2 Socket Numbers

The Enabler requires that the socket number be specified for the DAQP series PC card to be configured. Besides, the PC card must be inserted into the socket before invoking the Enabler.

For the DAQP series Enabler, the lowest socket number is always designated as socket 0, and the highest socket number as N-1 (assuming there are N sockets available). Some vendors number their sockets from 1 to N. If that is the case, the vendor's socket number minus 1 should be used in the "S" option for the DAQP series PC card Enabler.

4.3.3 Card and Socket Services Software

In order to use DAQP series PC card Enabler for DOS, the system must NOT be configured with Card and Socket Services software. If a Card and Socket Services software is installed, the Enabler may interfere with its operation and the devices it controls. Therefore, use DAQP series Client Driver and Enabler exclusively.

4.4 WHERE TO GO FROM HERE

The DAQP series PC card is now configured and ready for use. Depending on the type of application software to be used, the user may wish to review one or more of the following:

1. Chapter 5 of this document provides a basic theory of operation of the adapter for users who wish to learn the technical details about the operation of the DAQP series PC card.
2. For users who want to program the adapter with direct I/O transfers to the PC card's register set, chapter 7 provides an address map and a detailed description of each I/O register.
3. Users who would like to write custom application software without programming the DAQP series PC card directly should consult the DAQDRIVE software reference manual. DAQDRIVE provides a library of data acquisition subroutines for various data acquisition adapters and is included free of charge with the DAQP series PC card.
4. For turn-key data acquisition software (i.e. LabTech NoteBook, SnapMaster, LabView and TestPoint) consult the documentation provided by the software manufacturer.

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5. THEORY OF OPERATION

The DAQP series PC card consists of 8 differential or 16 single-ended analog input channels, each has a bipolar input range of ±10V, ±5V, ±2.5V, or ±1.25V (programmable gain of 1, 2, 4 or 8). The A/D converter, either 12 -bit or 16-bit, can be operated at its top speed of 100,000 samples per second (10 µs per sample).

The A/D converter uses left-justified 2's complement coding. For the 16-bit version, its output ranges from -32768 to 32767 as usual. However, the 12-bit version will have its 12-bit result occupying the most significant 12 bits, and padding its least significant 4 bits with all '0' to make a 16-bit output word for each converted input sample.

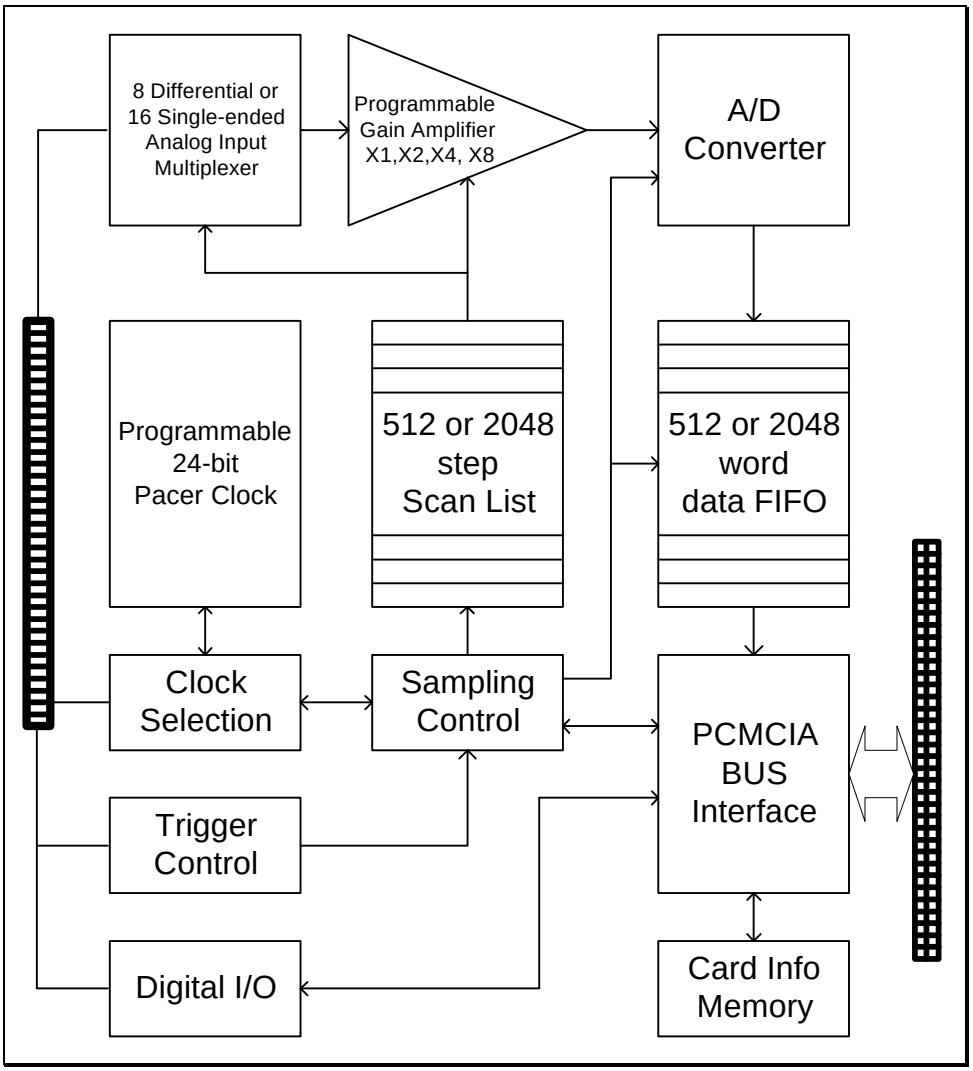

Figure 2 : DAQP Series Data Acquisition System Block Diagram

The DAQP series PC card can be operated as an I/O device, occupying eight consecutive bytes in the I/O address space. It can also be configured to operate via memory mapped I/O. It fully complies with the PCMCIA standard 2.10 as a type II card. The card does not have any jumpers or DIP switches, all of its configurable features are programmable.

Functionally, the DAQP series PC card consists of the following components: the DC/DC power supply, analog input multiplexer, programmable gain control, A/D converter, data FIFO, scan list, trigger control, pacer clock, interrupt & status, digital I/O, as well as the associated control circuits.

5.1 DC/DC POWER SUPPLY

The DAQP series PC card uses standard 5 volt power supply for its digital circuit. The ± 15 volt power supplies are used for the analog front end, and the analog +5 volt power supply for the A/D converter. All of them are generated by a DC/DC converter off the +5 digital input power supply from the PCMCIA connector. The DC/DC converter takes 140 mA, 78% of the 180 mA total load current, from the input power supply.

According to the new PCMCIA specification, any card that takes more than 100 mA must not be blindly turned on when the card is inserted, until it is intentionally accessed (by writing to the card configuration and option register, or its allocated I/O space). The DAQP series PC card will support the new specification by providing a unique power down mode control. When the card is first plugged in, powered up or reset, the DC/DC converter will be shut off, such that only the digital portion is up and running, taking only 40 mA from the input +5 power supply. The user has the option of reading the card information memory, where the maximum power consumption is listed for reference, and then decide whether to wake it up or not. If required, the card can be put into full powered mode the first time when its PCMCIA configuration and option register (COR) is written by the software.

After the card has been put into full powered mode for the first time by writing the PCMCIA configuration and option register, the card can be put into powered down mode (or full powered mode) by writing a ‘1’ (or ‘0’) into bit 2 (the power down bit, which is zero at reset or power up) of the PCMCIA auxiliary control register.

Please refer to chapter6 for more information about the PCMCIA configuration and option register (COR) , card configuration and status register (CCSR), and etc.

5.2 ANALOG INPUT MULTIPLEXER

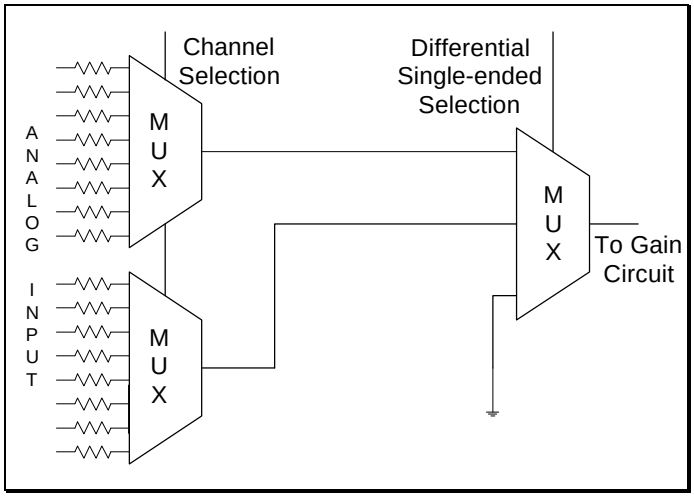

Figure 3 : Analog Input Circuit

The differential or single-ended configuration is determined by bit 6 of the high byte in the scan list entry. A '1' selects differential, while a '0' selects single-ended. The expansion cards can only be used on single-ended channels. It is strongly recommended that the single-ended/differential selection be the same for all the internal channels (e.g., all 8 channels as differential, or all 16 channels as single-ended). Having some channels configured as single-ended and others as differential, possible as it is, might cause confusion and unexpected signal errors.

In differential configuration, there are at most 8 channels. However, if the user specifies channel 8 to 15 in differential configuration, it only means to short the inputs to ground for system offset measurement. The readings taken under such a circumstance can be used for offset correction.

The input multiplexers have the built-in protection against over-voltage when the board is powered on AND when it is powered down. The protection mechanism will isolate the input from the rest of the board, as long as the input voltage is within the protection range of ± 30 volt.

5.3 PROGRAMMABLE GAIN CONTROL

The DAQP series PC card has an internal gain of 1, 2, 4, or 8. The gain can be changed "on the fly" from channel to channel when scanning through the channels. There is a programmable gain instrumentation amplifier with gains of 1, 2, 4, and 8. The internal gain selection is specified by the scan list entry (bit 4 and 5 of the high byte). The contents of these two bits will determine the gain of the analog front end.

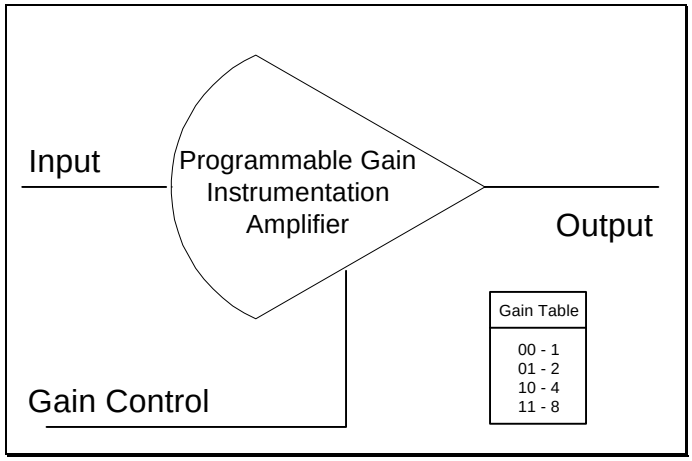

Figure 4 : Programmable Gain Control

The settling time of the analog front end meets the speed requirement. However, if the amplifier is saturated, it may need longer time to recover. That may cause distortion in the input signal to the A/D converter. It is always recommended that the amplifier saturation be avoided (use low gains, attenuate the input signal, and etc.).

5.4 SCAN LIST

One entry to the scan list contains a 16-bit word, or two 8-bit bytes. It specifies the internal channel selection and gain selection (in the high byte, or MSB), the external channel and gain selection (in the low byte, or LSB), as well as other control and configuration settings. Please refer to section 7.2 for the bit definition.

The external selections are used for channels on the expansion cards, while internal ones for channels on board the DAQP series PC card.

The expansion cards are not included as part of the DAQP series data acquisition system. However, they can be purchased separately from your vendor.

The number of entries in the scan list ranges from 1 to 512 (standard) or 2048 (with 2K option). There are no dependencies implied among the entries of the scan list. The user may choose any valid gain combinations for any channel, internal or external. The channels can be scanned in any order as required, repeated or not, with the same or a different gain for each entry.

The scan list has to be flushed before programming. The integrity of each entry has to be guaranteed. In other words, there must be even number of bytes programmed into the scan list, with the low byte sitting at an even offset followed by the high byte. Otherwise the result of channel scanning will be unpredictable.

It is strongly recommended that the differential/single-ended control bit (at bit 14, MSB) be programmed the same for all the entries in the scan list, which is most likely the case for normal operations. On the other hand, single-ended

configuration should be selected if there is one or more expansion cards connected to the DAQP series PC card.

The synchronous sample hold bit (at bit 6, LSB) is reserved for the expansion cards.

The first channel flag (bit 7, LSB) has to be set for the first (and ONLY the first) entry of the scan list. The DAQP series PC card hardware relies on this bit to tell the end (or the start) of the scan. In normal operations, the PC card starts one scan when a trigger comes (be it a software trigger or TTL trigger in one-shot mode, or the sampling pulse triggers from the pacer clock in continuous mode). During the scan, each entry in the scan list will be processed until the one that has the first channel flag set to '1'. The hardware stops the scanning and waits for the next trigger. However, the scan will be repeated forever if none of the entries has the flag set to '1'. On the other hand, if more than one entries have the flag set to '1', the scan list will then be chopped into pieces. Each piece requires a trigger to run through. Should the flag be set to '1' on an entry other than the first, a "starting offset" will be introduced to the scan list such that, for all but the first scan, the channel scanning will start from the one that has the flag set to '1', run through the list, turn around and end at the one before it. Useful as it might be for diagnosis or special applications, the abnormal way of setting the first channel flag should be avoided unless absolutely necessary.

5.5 TRIGGER CIRCUIT

As stated in the description of the control register (base + 2) in section 3.7, the DAQP series PC card can be triggered by the software (or an internal trigger as compared to that coming from an external TTL signal), the external TTL signal, or the pacer clock. For the external TTL trigger, an active trigger edge can be selected for either the low-to-high transition or the high-to-low transition.

In one-shot trigger mode, one trigger, either internal or external, will start one and only one scan of all the channels specified in the scan list. The pacer clock does not have any effect in this mode (it is good practice to program the pacer clock with a divisor greater that 2). Multiple scans can be realized by issuing (or receiving) multiple triggers.

In continuous trigger mode, the software or TTL trigger will start a series of scans, in which the first one is initiated immediately on receiving the trigger, while the rest are carried out each time the pacer clock fires. The process will continue until an A/D stop command (please refer to section 3.7 for description of sending commands to the DAQP series PC card) is received.

If the internal trigger (or the software trigger) is selected, the trig/arm command will serve as a trigger as soon as it is received by the PC card. For the external trigger source, the same command will be taken as an arm command, which arms the PC card such that the first proper trigger edge since the receiving of the arm command will serve as the trigger. Any trigger edges before the first one will be

ignored. Unexpected edge transitions during the configuration of the trigger source and edge will not be taken as triggers as long as the PC card is not armed.

5.6 A/D CONVERTER AND DATA FIFO

The DAQP series PC card always assumes a bipolar input range of ±10V if the gain is one. The output data format will always be in 2's complement (and left justified for 12-bit versions). The data acquisition time of the A/D converter is 2 µs while its conversion time no more than 8 µs. The output of the A/D converter is fed into the data FIFO providing data buffering of up to 512 (standard) or 2048 (with 2K option) samples.

The hardware design guarantees that the A/D converter, once triggered, will do conversion for every analog input channel specified in the scan list at the specified scan speed and feed the results into the data FIFO. In between scans, the PC card waits until another trigger comes in (one-shot mode) or the pacer clock fires (continuous mode).

The data FIFO has two programmable thresholds, one for almost full and the other for almost empty. The DAQP series PC card only uses the almost full threshold and ignores the other one. Please refer to section 7.2 and 7.7 for the detail about threshold programming.

The data FIFO should always be flushed prior to the arm/trig command starting the data acquisition. When the FIFO is flushed, or emptied by the host reading all of its content, the FIFO empty flag will be set to '1'. As long as there is one or more samples left in the data FIFO, the empty flag will be set to '0'.

When the number of data samples in the FIFO becomes greater than the programmed almost full threshold, the almost full flag will be set to '1'. When the number becomes less than or equal to the specified almost full threshold, the flag will be set to '0'. On power up or reset, the threshold is defaulted to 7 bytes to full (3.5 samples). ***Correct setting of the threshold will help achieve the optimal performance of the card.***

When the FIFO is full, the FIFO full flag will be set, and no more samples can be written into the FIFO. At the end of each scan, the DAQP series PC card will set the data lost flag if the data FIFO is already full. This flag will not be set before or during the scan, but at the end of it. Once the flag is set, it will not be cleared until the status register is read.

5.7 INTERRUPT AND STATUS

The DAQP series PC card has two interrupt sources, the end-of-scan (EOS) interrupt and the FIFO threshold interrupt. The control register (base + 2, write only) has two bits to enable or disable either one of the interrupts independently. However, it is strongly recommended that the two interrupt be used exclusively.

When the EOS interrupt is enabled, an interrupt will be sent to the host at the end of each scan of the channel list. If there is only one channel in the scan list, the EOS interrupt is reduced to an EOC (end-of-conversion) interrupt.

The FIFO threshold interrupt, when enabled, will be sent to the host when the almost full flag is set. The host can then use the "string input" instruction to move a block of samples from the FIFO.

The EOS and FIFO threshold event bits in the status register (base + 2, read only) will be set whenever the corresponding event happens. These bits can be used for indicating the source of the interrupt. Once set, the event bits will not be cleared until the host reads the status register.

5.8 DIGITAL I/O

The DAQP series PC card has one digital input port (base + 3, read only) of four bits (bit 0-3), and one digital output port (base + 3, write only) of four output bits (bit 0-3). The output port is latched, but the input port is not.

Four input lines are connected to the digital input port, each representing one bit in the port. When reading the digital input port, the CURRENT status of the digital input lines are returned to the host.

All of the four input lines are shared with other functions. Bit 0 will be shared as the external trigger input, while bit 2 is shared as the external clock input. Bit 1 and 3 are taken over as the external gain selection lines if there is one or more expansion card connected and the expansion bit in the control register is set to '1'. Nevertheless, the current status of the digital input lines will always be returned when the host reads the digital input port, no matter the lines are shared or not.

The four digital output lines will be taken over as the external channel selection lines if the expansion bit is set in the control register. In that case, the digital output lines will be driven by the external channel selection bits of the current scan list entry (see the description of the scan list). Otherwise, they will be connected to the latched bit 0-3 of the digital output port.

5.9 A/D STATE MACHINE

The DAQP series PC card has an internal state machine (Figure 5) that controls the A/D operation. Please refer to section 7.7 for details about sending control commands to the PC card.

The state machine defaults to S0 after power up or reset. The normal state flow would be first S0 to S3, initiated by a scan list (queue) flush command (RSTQ). Then the queue must be programmed by writing into the queue (base + 1). With the queue being programmed, the next step is moving the state machine from S3 back to S0. This is done by issuing a flush data FIFO command (RSTF), which sets up the gain and channel selections for the first channel in the scan list, and waiting for a trigger to start the scan. When the trigger (ADCLK) comes, the state

machine moves from S0 to S1, and the A/D conversion will be started once it is moved to S1. The state machine will wait at S2 until the conversion is done. At that time it moves to S4, where the A/D conversion result is written into the data FIFO. The scan rate is determined by the time the state machine moves from S1 to S4, which can be programmed as either 10, 20 or 40μs. If there are more channels to scan in the list, the state machine will skip to S1 for another conversion loop. Otherwise it will return to S0, waiting for another trigger (or a sampling pulse from the pacer clock if it is in the continuous trigger mode). Any time during data acquisition, an A/D stop command will clear RUN to zero and eventually stop the data acquisition by moving the state machine back to S0.

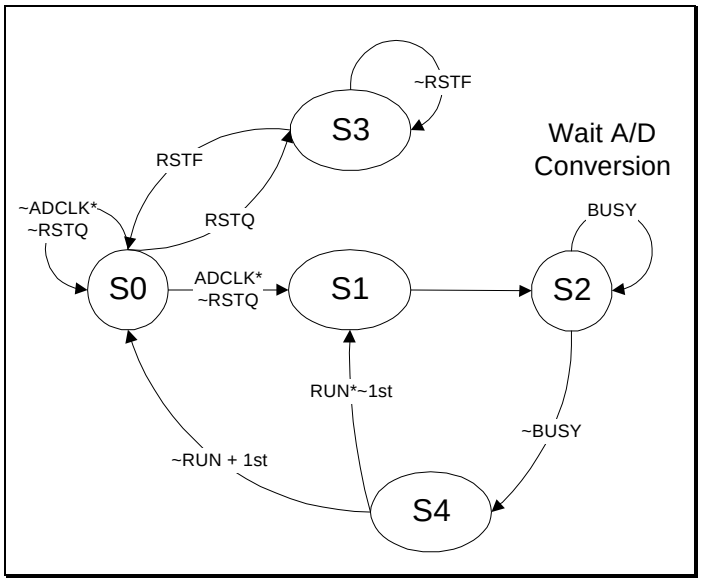

Figure 5 : The State Transition Diagram of A/D Conversion Process

It is important that the first trip of S0-S3-S0 be followed as described above. The user has to issue two commands to the PC card. The flush scan list command (RSTQ) and then the flush data FIFO command (RSTF). In between is the time for programming the scan list. Once the flush data FIFO command is issued, the PC card will prepare the first channel in the scan list, and then back to state S0 waiting for the first trigger. It also guarantees that the scan list and the data FIFO are flushed properly for the expected data acquisition.

ATTENTION *Anytime the data FIFO is flushed, the default threshold setting will be restored (7 bytes to full) by the hardware. The data FIFO threshold should always be programmed after the flushing if the required threshold is different from the default one.*

6. PCMCIA INTERFACE

Information in this section is provided for those who needs low level PCMCIA interface details to the DAQP series PC card. The client driver or the enabler that comes with the PC card will be sufficient for most applications.

The DAQP series PC card performs data acquisition for all host computers equipped with a version 2.1 compliant PCMCIA interface. As a PC card, a name that has been given to all the PCMCIA interface cards, the PC card has a form factor of type II (5 mm thick).

Thanks to the PCMCIA interface, the PC card is highly flexible with respect to addressing and interrupt level use. It can be configured either as a memory only interface or as an I/O interface, and be powered up or down with the help of the PCMCIA card and socket services. The DAQP series PC card provides a single interrupt that is routable to any system interrupt via the PCMCIA socket controller.

There are two sets of registers on the DAQP series PC card, the configuration registers and program registers.

The configuration registers are those as defined in the PCMCIA 2.1 specification. The PCMCIA configuration registers are located in the PC card's configuration space at offset 8000H. Configuration space also contains the Card Information Structure (CIS). This memory is located at offset 0000H in the configuration space. The CIS memory contains information about the PC card as defined by the PCMCIA 2.1 specification. It is recommended that the configuration, power up/down control of the PC card be carried out through the standard card and socket services, though they can be realized with an enabler.

Program registers are the registers that fall under program control and belong to the DAQP series PC card. The I/O location of these registers are controlled by the PCMCIA socket configuration and by the contents of the PCMCIA configuration registers. Please see the description in chapter 7 for detail.

Two PCMCIA configuration registers are supported by the DAQP series PC card, the Configuration Option Register and the Card Configuration and Status Register.

Table 2. PCMCIA Configuration Registers

Offset	Access	Description
0x8000	R/W	Configuration Option Register
0x8002	R/W	Card Configuration and Status Register

6.1 Configuration and Option Register (COR)

Bits 7 and 6 of the Configuration Option Register are defined by the PCMCIA standard as the SRESET and the LevlREQ Bits. A '1' written into the SRESET bit puts the card into a reset state, while a '0' moves it out of the reset state. When the card is in reset state, it behaves as if a hardware reset is received from the host. The LevlREQ bit controls the type of interrupt signal generated by the PC card. Setting the Configuration Index bits to '0' makes the PC card a memory only card (accessed only by memory read/write operations), while setting to '1' enables the card to be a standard I/O card.

Table 3. Bit Definition of COR

Bit	Name	Description
7	SRESET	1 = Put the card into reset state 0 = Get out of reset state
6	LevlReq	1 = Level mode interrupt 0 = Edge mode interrupt
5-0	Index Bits	000000 = Memory mode 000001 = I/O mode

6.2 Card Configuration and Status Register (CCSR)

The DAQP series PC card uses two bits in this register. When bit 1 is set to '1', it indicates a pending interrupt. The bit will remain as '1' until the software clears the interrupt source. Bit 2 is used for power down control. A '1' set to this bit will put the card into power down mode, while a '0' brings it back to full powered mode. The rest of the bits are not used.

Table 4. Bit Definition of CCSR

Bit	Name	Description
7--3	Not Used	Reserved, all '0' when writing and reading
2	PwrDwn	1 = Power down mode 0 = Full powered mode
1	Intr	1 = Interrupt pending 0 = No interrupt pending
0	Reserved	Reserved as '0'

7. I/O REGISTERS

The DAQP series PC card uses eight consecutive I/O locations within the system I/O address space. The base address of the adapter is determined by the Client Driver or Enabler as discussed in sections 3 and 4. The eight I/O locations are used by the PC card as summarized in the following table.

Table 5. DAQP Series PC Card Register Map

Address Lines (A2A1A0)	I/O Address	Port Access	Register Description
000	base + 0	Read/Write	Data FIFO
001	base + 1	Write Only	Scan List (Queue)
010	base + 2	Write Read	Control Register Status Register
011	base + 3	Write Read	Digital Output Register Digital Input Register
100	base + 4	Write Only	Pacer Clock, low byte
101	base + 5	Write Only	Pacer Clock, middle byte
110	base + 6	Write Only	Pacer Clock, high byte
111	base + 7	Write Only	Auxiliary Control Register

All the registers are 8-bit wide. Each register will be discussed in detail in the following sections.

7.1 Data FIFO Register (base + 0)

The data FIFO register can be considered as the access port to the data FIFO, which can hold up to 512 (standard) or 2048 (with 2K option) data words of the A/D conversion result. The port is also used for programming the data FIFO thresholds, as explained later in this section.

> **NOTE**: *Although the data FIFO register is 8-bit wide, it is strongly recommended that the register be accessed as a 16-bit word to guarantee the integrity. The low byte (LSB, or the least significant byte) should always be accessed first, followed by the high byte (MSB, or the most significant byte).*

Two consecutive bytes should be read from (written into) the port each time it is accessed. The following table illustrates the bit allocation.

Table 6. Data FIFO Register Bit Allocation

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
LSB	D7	D6	D5	D4	D3	D2	D1	D0
MSB	D15	D14	D13	D12	D11	D10	D9	D8

7.1.1 Data FIFO Operation Modes

Depending on the mode of operation, the 16-bit word read from or written into the register has different meanings, as described in the following table.

Table 7. Data FIFO Operation Mode

Mode	**Selection Bit**	**A/D**	**Access**	**Operation**
0	0, threshold	Idle	Read Write	Verify data FIFO threshold Program data FIFO threshold
1	1, data FIFO	Idle	Read Write	Read data FIFO Write data FIFO (diagnosis)
2	0, threshold	Run	Read Write	Verify data FIFO threshold Not allowed
3	1, data FIFO	Run	Read Write	Read data FIFO Not allowed

The 'selection bit' in Table 7 is also called the 'program/access' control bit, as defined in the auxiliary control register (base + 7). Please refer to section 7.7 for details of setting the bit and issuing commands to change the status of the A/D conversion (from scan to idle or vice versa).

Mode 0 is the FIFO program mode, under which the two consecutive words (four bytes) written into the register address will set the almost full and almost empty thresholds (in bytes). The first word specifies the almost empty threshold (not used, can be set to anything), while the second word determines the almost full threshold. The threshold should be set to a value from 1 to FIFO size minus 1 (default is 7 when reset or power up).

Table 8. Data FIFO Threshold Setting

Threshold	Default	Threshold Range	Suggested Value
Almost Empty	7	Irrelevant	Irrelevant
Almost Full	7 7	1..1023 (standard) 1..4095 (2K option)	512 2048

Mode 1 is the FIFO test mode, in which the data bytes will be written into the data FIFO, and read back from it. The FIFO flags (the FIFO empty, almost full, and full flags, see description of the status register at base + 2 for detail) will change according to the data bytes available in the data FIFO and the configured threshold.

Mode 2 should be avoided. The data bytes can not be written into the FIFO under this mode, while the bytes read from the FIFO will be the same as in mode 0.

Mode 3 is the data transfer mode. Data bytes will be written into the FIFO by the A/D converter, while the data byte read from the address is the first available byte in the data FIFO if it is not empty, otherwise the most recent byte written into the FIFO will be returned. The data FIFO register is read-only under this mode, i.e., the user can NOT write data bytes into the data FIFO through I/O instructions.

7.1.2 Mode Setting

The FIFO operation mode setting is always initiated with the data FIFO flush command (see auxiliary control register in section 7.7) with the access/program bit set to '0' (bit 0 at base + 7) BEFORE the data acquisition is started. This will bring it to mode 0 (threshold setting mode). After the threshold is programmed or verified, set the bit to '1' so that the following read/write operation to the FIFO will be data access operation.

The DAQP series PC card is in idle mode before it is triggered into the run mode. For one-shot operation, the PC card will be set to run mode after it receives the

trigger signal. It will not return to the idle mode until the specified scan list is completed, or a A/D stop command (see section 7.7 for detail) is received. For continuous trigger operation, the PC card will stay in run mode after being triggered until an A/D stop command is received.

7.1.3 FIFO Flags

When reading the register under mode 1 or 3, the first available data byte from the data FIFO will be returned if it is not empty, otherwise the returned byte is not defined. The FIFO empty flag will be set immediately after the last byte is read from the FIFO, while the FIFO full flag will be cleared after reading the data FIFO register, provided that there are no more data bytes written into the FIFO by the A/D converter under mode 1 or 3. The same will happen to the FIFO almost full flag, if the data bytes available in the FIFO are less than the almost full threshold.

Table 9. Data FIFO Flag Status

Data bytes in FIFO	Empty	Almost Full	Full
0	True	False	False
1 to (Threshold - 1)	False	False	False
Threshold to (FIFO size - 1)	False	True	False
FIFO size (either 1024 or 4096)	False	True	True

where “Threshold” is the almost full threshold as explained before, and “FIFO size” is measured in bytes, either 1024 (standard) or 4096 (with 2K option).

7.2 Scan List Queue Register (base + 1)

The Scan List Queue Register can be considered as the access port to the scan list queue, which can hold up to 512 entries (each has two bytes), each specifying an analog input channel and its associated gain, as well as other settings.

NOTE: *Although the scan list queue register is 8-bit wide, it is* ***required*** *that the register be accessed as a 16-bit word to guarantee the integrity. The low byte (LSB, or the least significant byte) should always be accessed first, followed by the high byte (MSB, or the most significant byte).*

The bit definition of an entry to the scan list queue is explained in the following table.

Table 10. Bit Definition of the Scan List Queue Entry

Bit	Byte	Definition	Explanation
15	MSB	Reserved	as 0
14	MSB	Analog input mode	1/0 : differential/single-ended
13-12	MSB	Internal gain selection	00/01/10/11 : 1/2/4/8
11-8	MSB	Internal channel selection	0000..1111 : channel 0..15
7	LSB	Starting channel mark	Set to '1' for the 1st entry in the list Set to '0' for all the rest entries
6	LSB	Reserved	for expansion cards (as SSH)
5-4	LSB	External gain selection	00/01/10/11 : 1/2/4/8 (or 1/10/100/1000)
3-0	LSB	External channel selection	0000..1111 : channel 0..15

7.2.1 Scan List Queue Programming

The scan list queue has to be programmed when the DAQP series PC card is idle. Each queue entry contains two bytes as described above. The integrity of the entry has to be guaranteed. The scan list queue is write only.

The scan list queue should be flushed first before writing any entries into it. Please refer to the auxiliary control register about scan list queue reset.

The first entry of the queue should have bit 7 (LSB) set to '1' as the first channel mark. All the rest entries, if any, should have the bit set to '0'.

The synchronous sample hold bit (LSB) is not used by PC card. It is reserved for the expansion cards.

Example 1.

The following entries to the queue specify a scan list of 3 single-ended internal channels, 0, 12, and 7 with gain of 2 for channel 0, gain of 4 for channel 12 and 7:

Table 11. Scan List Queue Programming Example 1

Entry	Binary	Hex	Explanation
1	0001 0000 1000 0000	0180	Select channel 0, gain 2, 1st entry
2	0010 1100 0000 0000	2C00	Select channel 12, gain 4
3	0010 0111 0000 0000	2700	Select channel 7, gain 4

Example 2.

The following entries to the queue specify a scan list of 4 differential internal channels, 2, 1, 6 and 7 with gain of 1 for all the channels:

Table 12. Scan List Queue Programming Example 2

Entry	Binary	Hex	Explanation
1	0100 0010 1000 0000	4280	Select channel 2, gain 1, 1st entry
2	0100 0001 0000 0000	4100	Select channel 1, gain 1
3	0100 0110 0000 0000	4600	Select channel 6, gain 1
4	0100 0111 0000 0000	4700	Select channel 7, gain 1

7.2.2 Channel Configuration

The bit 5 and 4 (LSB) in a queue entry specify the gain on the external expansion card for the external channel selected by bit 3-0 of the same byte. Each expansion card has up to 16 channels (0, 1, 2, ..., 15). Each channel may have a gain of 1, 2, 4, 8 if it is a low gain card, or 1, 10, 100, 1000 if it is a high gain card.

If there is no expansion card for the specified internal channel, the external channel and gain selection in the LSB will be ignored. However, the first channel mark on bit 7 should always be set properly.

The internal channel is selected by bit 8-11 (MSB), while the internal gain for the selected channel is specified by bit 12 and 13 (MSB). The internal gain can only be 1, 2, 4, or 8.

Bit 14 (MSB) determines whether the input is differential (1) or single-ended (0). There are 16 singled-ended channels, but only 8 differential channels. This bit should always be set to ‘0’ if the selected internal channel is connected to an expansion card, because the output from the expansion cards is always single-ended.

Bit 15 (MSB) is not used by the DAQP series PC card. It should be set to ‘0’.

7.2.3 Analog Input Offset Correction

The input to the A/D converter will be shorted to ground if bit 14 (MSB) is set to ‘1’ while the internal channel selection of bit 8-11 specifies internal channel 8 or above. This can be used for analog input offset correction.

7.3 Control Register (base + 2, write)

The control register specifies the pacer clock source and pre-scaler, the expansion mode, interrupt enable control and the trigger control.

Table 13. Control Register Bit Definition

Bit	Function	Explanation
7-6	Pacer clock source and pre-scaler	00 : External clock 01 : Internal, 5 MHz 10 : Internal, 1 MHz 11 : Internal, 100 kHz
5	Expansion mode	0/1 : disable/enable
4	EOS interrupt	0/1 : disable/enable
3	FIFO interrupt	0/1 : disable/enable
2	Trigger mode	0/1 : one-shot/continuous
1	Trigger source	0/1 : internal/external
0	Trigger edge	0/1 : rising/falling

7.3.1 Clock Source

The external clock source, if selected, must not exceed 5 MHz with a minimum pulse width of 200 ns. The external clock frequency can be as low as DC, and there is no limit on maximum pulse width.

7.3.2 Expansion Mode

Bit 5 has to be set to '1' if there is one (or more) expansion card connected to the DAQP series PC card. This also means that all of the digital output lines (bit 0 to 3) will be used as external channel selection and two of the four digital input lines (bit 1 and 3) will be used as external gain selection.

7.3.3 Interrupt Enable

Bit 4 and 3 are used for interrupt enable control. The end-of-scan (EOS) interrupt will be enabled (disabled) by setting bit 4 to '1' ('0'). Setting bit 3 to '1' ('0') will enable (disable) the data FIFO interrupt when the A/D data FIFO becomes almost full (data available in the FIFO passes the almost full threshold). Since the EOS and FIFO threshold events are latched into the status register, temporarily disabling the interrupt and then enabling it will not lose an interrupt, as long as there are no repeated events during the time the interrupt is disabled.

7.3.4 Trigger Mode

Bit 2 determines the trigger mode. It is set to '0' for the one-shot mode, where each trigger signal, internal or external, will start one scan of input analog channels specified by the scan list. Bit 2 should be set to '1' for the continuous trigger mode, in which the trigger signal, internal or external, will start the first scan of the input analog channels specified by the scan list, and the pacer clock will then initiate the subsequent scans each time it fires, until the stop A/D command is received.

7.3.5 Trigger Source

Bit 1 specifies the trigger source. It is set to '1' for external trigger (TTL trigger), and '0' for internal trigger (software trigger). When it is set to internal trigger, the trigger edge selection can be ignored. The external trigger signal shares the same pin on the interface connector with the digital input bit 0.

7.3.6 Trigger Edge

Bit 0 selects the external trigger edge. Falling edge of the external trigger signal will be chosen as the trigger edge if the bit is set to '1', otherwise the rising edge is selected. The edge selection will be ignored if the internal trigger source is specified.

7.4 Status Register (base + 2, read)

The status register is read only. It shares the same offset as the control register. It reports data FIFO flag status, interrupt status and A/D conversion status.

Table 14. Status Register Bit Definition

Bit	Status	Explanation
7	Scanning status	0/1 : busy / idle
6	Triggered status	0/1 : no / yes
5	Data lost event	0/1 : no / yes
4	End of scan event	0/1 : no / yes
3	FIFO threshold event	0/1 : no / yes
2	Data FIFO full	0/1 : false / true
1	Data FIFO almost full	0/1 : false / true
0	Data FIFO empty	0/1 : false / true

Bit 7 shows the scanning status. It is '0' when the PC card is in the process of scanning the input channels specified by the scan list, and '1' when it is done.

A '1' at bit 6 indicates that the PC card has been triggered and is doing the data acquisition (busy). Bit 6 is '0' means it is waiting for a trigger (idle).

Bit 3, 4 and 5 are the event latches. When an event is detected, the corresponding bit will be set to '1' until the host reads the status register, which clears all the event bits to '0'. Bit 5 is used for data lost event, bit 4 for end-of-scan (EOS) and bit 3 for the FIFO threshold event. When the corresponding interrupt is enabled, a '1' in bit 3 (or bit 4) will also cause an interrupt.

Bit 0, 1 and 2 are the data FIFO flags.

7.5 Digital I/O Register

7.5.1 Digital Output

The four digital output lines share the same pins on the interface connector with the four external channel selection bits. When using the expansion cards, bit 5 of the control register (base + 2) should be set to '1', such that the four lines will be driven by the external channel selection bits from the scan FIFO. On the other hand, the four output lines will be driven by the values in bit 0 to 3 latched during the last write operation if bit 5 of the control register is set to '0' (default after reset). In other words, the digital output bits will only be valid when DAQP series PC card is NOT in expansion mode. They will be ignored otherwise.

Table 15. Digital Output Register Bit Definition

Bits	Normal Mode	Expansion Mode
0-3	Digital output bit 0-3	Ignored, the four output lines will be driven by the external channel selection bits in the scan list FIFO
4-7	Reserved as all '0'	Ignored

7.5.2 Digital Input

As mentioned before, two of the digital input lines are shared with external trigger (bit 0) and external clock (bit 2). The other two lines will also be taken for external gain control in the expansion mode (if bit 2 of the control register is set to '1', see section7.3). The digital input lines are not latched. The following table shows what will be returned when reading this port.

Although the digital input lines are also used as external trigger, external clock and the external gain selection, the current status of these lines will always be returned

when reading the port. However, the line status has nothing to do with the digital output register, whose contents can NOT be read back directly, even though they share the same port offset with the digital input register.

Table 16. Digital Input Register Bit Definition

Bits	Normal Mode	Expansion Mode
0	Digital input bit 0, also serve as external trigger	The same as in normal mode
1	Digital input bit 1	External gain select, low bit
2	Digital input bit 2, also serve as external clock	The same as in normal mode
3	Digital input bit 3	External gain select, high bit
4-7	All '0'	All '0'

7.6 Pacer Clock (base + 4, + 5, + 6)

The pacer clock is actually a 24-bit auto-reload frequency divider. It contains a 24-bit divisor register, a 24-bit counter, an internal clock pre-scaler and a clock source multiplexer, as shown in the block diagram below:

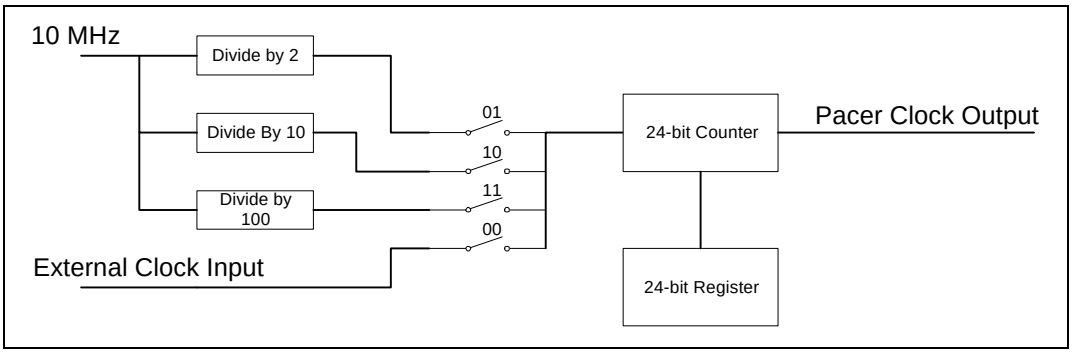

Figure 6. Pacer Clock Block Diagram

The clock source selection is specified by bit 6 and 7 in the control register (base + 2, see section7.3). The 24-bit register occupies 3 ports, in which the low byte is located at base + 3, the middle byte at base + 4, and the high byte at base + 5. All three registers are write only. The pacer clock will not generate any clock pulse output until it is triggered (either by an internal software trigger or an external TTL trigger signal), and the trigger mode is NOT one-shot. In continuous mode, the trigger will serve as the first clock output pulse, and load the counter from the register. Then the counter will down count the input clock pulse until it is down to zero, an output clock pulse will then be generated and the counter will be reloaded. The pacer clock generation will continue until the DAQP series PC card

receives the stop command, represented by writing a '1' at bit 4 of the auxiliary control register (base + 7, see section 7.7).

The clock rate generated can be determined by (Source Frequency) / (Divisor Count + 1). For example, if the clock source is 100 kHz (internal clock, control register bit 7,6 = 11), the divisor count is 49, then the pacer clock output frequency will be 2 kHz. If an external clock source (control register bit 7,6 = 00) of 120 kHz is applied, and the divisor count is 39, the pacer clock will then be set at 3 kHz.

7.7 Auxiliary Control Register (base + 7)

The auxiliary control register is used for the program to send control commands to the DAQP series PC card. It also sets the data program/access mode for the data FIFO. The command bits (bit 4 to 7) are actually 'monostable' or self-cleared after the specified command function is completed. They do NOT need to be cleared. However, the data FIFO program/access bit is latched each time it is written.

Table 17. Auxiliary Control Register Bit Definition

Bit	Function	Explanation
7	Trigger/Arm command	1 = send trigger/arm, 0 = no action
6	Flush data FIFO command	1 = flush, 0 = no action
5	Flush scan list command	1 = flush, 0 = no action
4	Stop A/D command	1 = stop, 0 = no action
3	Reserved	as '0'
2-1	Scan rate selection	00 = 100, 01 = 50, 10 = 25 (kHz)
0	Data FIFO program/access	1 = data access, 0 = program threshold

7.7.1 Trigger/Arm Command

If the trigger source is internal (software trigger), writing a '1' at bit 7 will send a trigger to the PC card, and start A/D conversion process. If the trigger source is external (TTL trigger), writing a '1' to bit 7 will serve as an ARM command, which tells the PC card to look for the specified external trigger edge from the moment the ARM command is received. This command should never be issued together with the stop A/D command. The data acquisition will be initiated after this command is received. Only the stop A/D command can terminate the acquisition.

7.7.2 Flush Data FIFO Command

The data FIFO should be flushed BEFORE the data acquisition can be initiated by the trigger/arm command, but AFTER the scan list has been set up. The flush command may also be followed by FIFO threshold programming. After the FIFO is flushed, the FIFO empty flag will be set to '1' and the almost full and full flag reset to '0'. The flush FIFO command ALWAYS sets the FIFO thresholds to the default setting (7 bytes to full) at power up or reset.

ATTENTION*Anytime the data FIFO is flushed, the default threshold setting will be restored (7 bytes to full) by the hardware. The data FIFO threshold should always be programmed after the flushing if the required threshold is different from the default one.*

7.7.3 Flush Scan List Queue Command

The scan list queue needs flushing before it can be programmed. This command should be issued before the flush data FIFO command. The queue may have up to 512 (standard) or 2048 (with 2K option) word entries, each containing two bytes. It is the user's responsibility to guarantee the integrity of the entries. Please refer to the discussion on the scan list queue (base + 1) for more information about the scan list queue.

7.7.4 Stop A/D Command

Once the data acquisition is started by the trigger/arm command, it can only be stopped by receiving this command. As mentioned before, the two commands are exclusive. The stop A/D command should be issued as soon as the required data points are collected to prevent data FIFO overflow, which is the only flag to indicate data lost during the data acquisition process. Without the stop command, the A/D may still be running and filling data into the data FIFO whether it is filled up or not. When the data FIFO is full, it will ignore the data samples coming from the A/D converter.

7.7.5 Data FIFO Program/Access Control

The A/D data FIFO has two programmable thresholds, almost empty and almost full, and two associated flags. The almost empty threshold is not used, nor is the almost empty flag. By default, the thresholds are set to 7 bytes (7 to full and 7 to empty) when reset, powered up, or anytime the FIFO is flushed. It can be programmed to any value in between 1 to FIFO size - 1 (in bytes), according to the application. For example, it can be set to the length of the scan list, half to full or quarter to full, and etc.

To program the FIFO threshold, make sure the A/D has been stopped. Set this bit to '0' by writing an all '0' byte to the auxiliary control register. Then send a flush A/D FIFO command with the same bit setting by writing a byte of 40H (hex 40)

to the same register. This will put the FIFO into program mode. The following read/write operation will be directed to the threshold registers instead when accessing the data FIFO at base + 1. The 4 byte threshold setting should be written into the data FIFO by doing four consecutive write operations. Optionally, the threshold setting can be read back for verification by doing four consecutive read operations. The 4 byte threshold setting has the following format

Table 18. Data FIFO Threshold Setting

Byte No.	Definition	Valid Range
0	Low byte of the almost empty threshold	0..255
1	High byte of the almost empty threshold	0..3 (standard) 0..15 (2K option)
2	Low byte of the almost full threshold	0..255
3	High byte of the almost full threshold	0..3 (standard) 0..15 (2K option)

After the thresholds are programmed, set the access control bit to '1' by writing a byte of 01H into the auxiliary control register. This will make the following read/write operation to access the data bytes in the FIFO instead of its thresholds. It is recommended that the access control bit be set to '1' when sending other command (flush scan list, stop A/D, or trig/arm) to DAQP series PC card by writing into the auxiliary control register after programming the thresholds. A useful tip for safety operation is to set the bit to '0' only when flushing and programming the FIFO thresholds.

Although the almost empty threshold is never used, it has to be programmed because the four configuration bytes must be accessed as a whole entity.

7.7.6 Scan Rate Selection

Depending on the input mode and the gain selection, the analog front end may have different settling times. In order to keep the best performance, the DAQP series PC card allows the user to choose 3 different scanning rate by setting bit 2 and bit 3 while the start A/D command is issued. The default scanning rate is 100 kHz (bit 3-2 set to '00'). 50 kHz rate can selected by setting the bits to '01', and 25 kHz by setting them to '10'. Setting the bits as '11' is the same as '01'.

It is recommended that the scan rate setting be issued together with the trigger/arm command, and not changed during data acquisition. For example, writing 81H to the auxiliary control register will start the data acquisition with the scan rate set to 100 kHz (use 83H for 50 kHz and 85H for 25 kHz).

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8. I/O CONNECTIONS

The DAQP series PC card is fitted in with a 33-pin 0.8 mm shielded connector with the pin assignment shown in the figure below. A mating connector is available from AMP (order part number 558126-4).

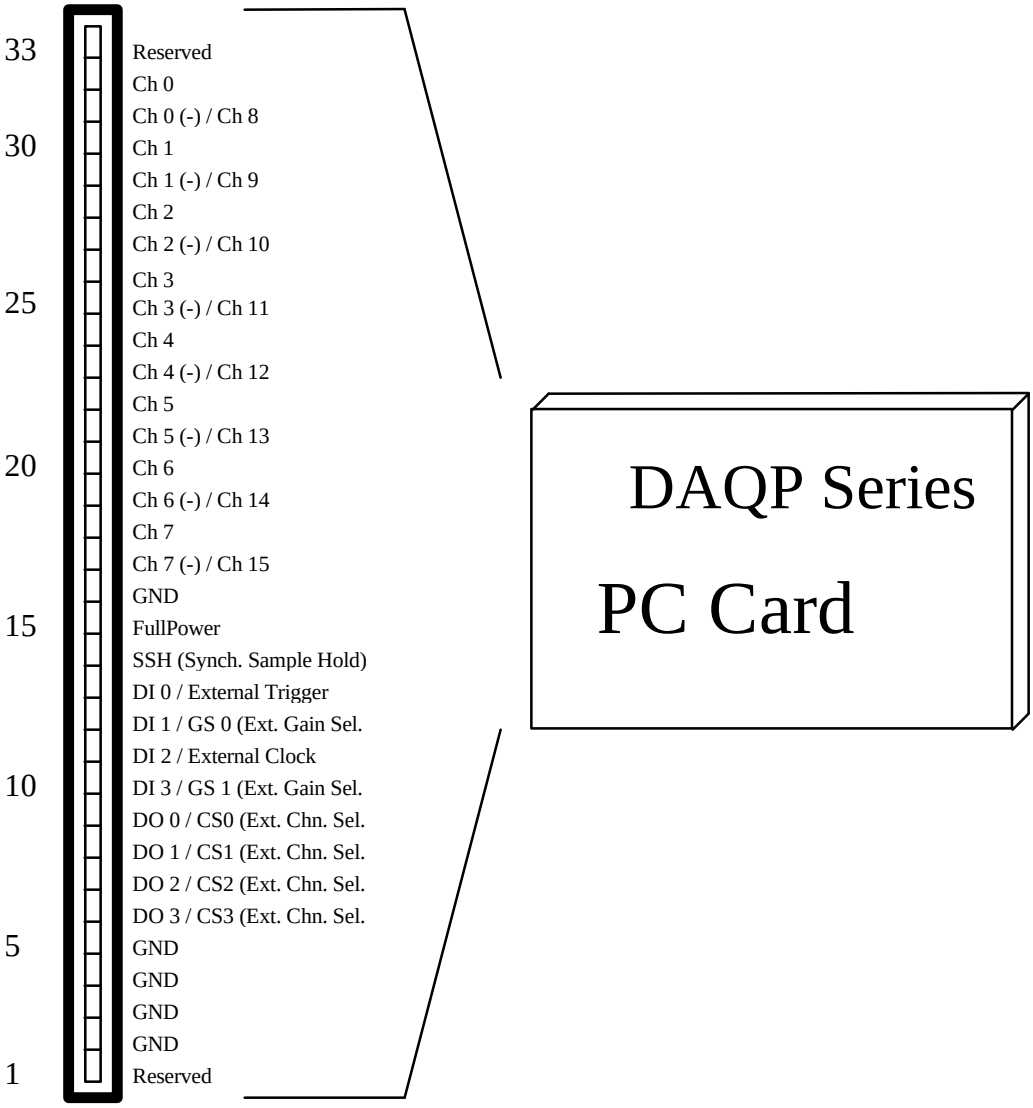

Figure 7. DAQP Series PC card AMP-33 Output Connector

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9. OPTIONAL ACCESSORIES

9.1 CABLE ASSEMBLY

Table 19. DAQP Series PC Card Cable Mapping

AMP-33	D-37	Name		Description
33	9	Reserved		For D/A output channel 0
32	37	Channel 0 (+)	Channel 0	A/D input, differential / single-ended
31	18	Channel 0 (-)	Channel 8	A/D input, differential / single-ended
30	36	Channel 1 (+)	Channel 1	A/D input, differential / single-ended
29	17	Channel 1 (-)	Channel 9	A/D input, differential / single-ended
28	35	Channel 2 (+)	Channel 2	A/D input, differential / single-ended
27	16	Channel 2 (-)	Channel 10	A/D input, differential / single-ended
26	34	Channel 3 (+)	Channel 3	A/D input, differential / single-ended
25	15	Channel 3 (-)	Channel 11	A/D input, differential / single-ended
24	33	Channel 4 (+)	Channel 4	A/D input, differential / single-ended
23	14	Channel 4 (-)	Channel 12	A/D input, differential / single-ended
22	32	Channel 5 (+)	Channel 5	A/D input, differential / single-ended
21	13	Channel 5 (-)	Channel 13	A/D input, differential / single-ended
20	31	Channel 6 (+)	Channel 6	A/D input, differential / single-ended
19	12	Channel 6 (-)	Channel 14	A/D input, differential / single-ended
18	30	Channel 7 (+)	Channel 7	A/D input, differential / single-ended
17	11	Channel 7 (-)	Channel 15	A/D input, differential / single-ended
16	29	GND		
15	10	FullPower (org. D/A 0 ref. in)		1/0 : Full power / Power down
14	26	SSH (org. D/A 1 ref. in)		Synchronous Sample Hold
13	25	Digital in bit 0 (shared)		External trigger (same as in DAS-16)
12	6	Digital in bit 1 (normal mode)		External gain, LSB (expansion mode)
11	24	Digital in bit 2 (shared)		External clock (org. DAS-16 Ctr 0 Gate)
10	5	Digital in bit 3 (normal mode)		External gain, MSB (expansion mode)
9	23	Digital out bit 0 (normal		External channel bit 0 (expansion mode)
8	4	Digital out bit 1 (normal		External channel bit 1 (expansion mode)
7	22	Digital out bit 2 (normal		External channel bit 2 (expansion mode)
6	3	Digital out bit 3 (normal		External channel bit 3 (expansion mode)
5	28	GND		
4	28	GND		
3	19	GND		
2	19	GND		
1	27	Reserved		D/A output channel 1

An optional cable assembly, part number CP-DAQP, is available for converting the PC card's 33-pin I/O connector to a standard D-37 connector (both male and female are available). The D-37 connector is compatible with the P-1 connector of the Keithley DAS-16™. The pin assignment of the D-37 is illustrated in the following figure.

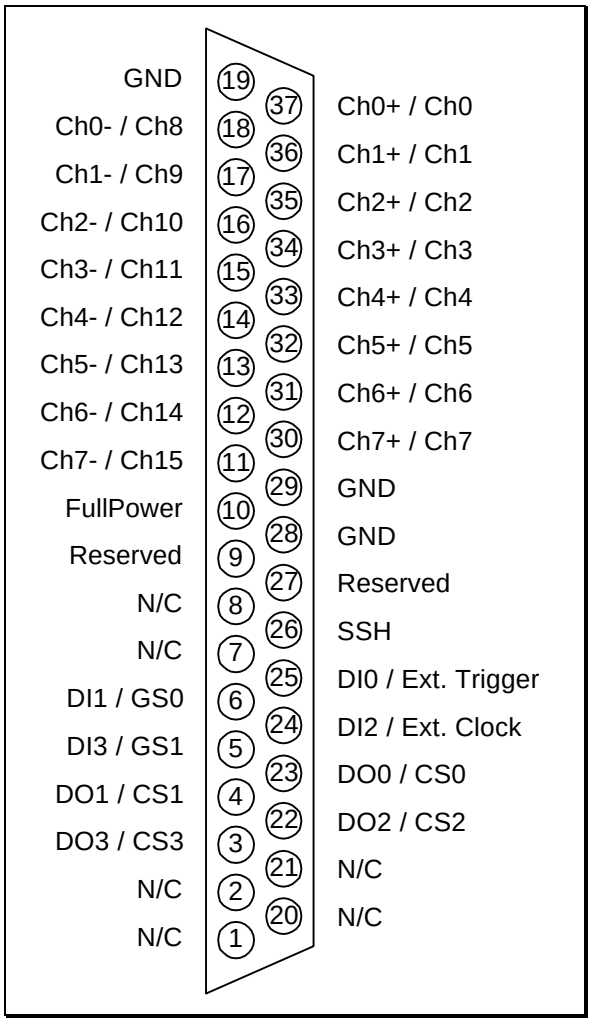

Figure 8. DAQP Series PC Card Optional D-37 Output Connector

9.2 UIO-37 SCREW TERMINAL ADAPTER BOX

The DAQP series PC card may also be equipped with an optional screw terminal box. It has a D-37 connector (both male and female are available), matching with the optional CP-DAQP cable assembly. Its part number is UIO-37. The box provides an easy way of connecting signals to the PC card. There are two rows of screw terminals. The first row (inside) goes from pin 1 to pin 19, while the second row (outside) from pin 20 to pin 37, as illustrated in the following figure.

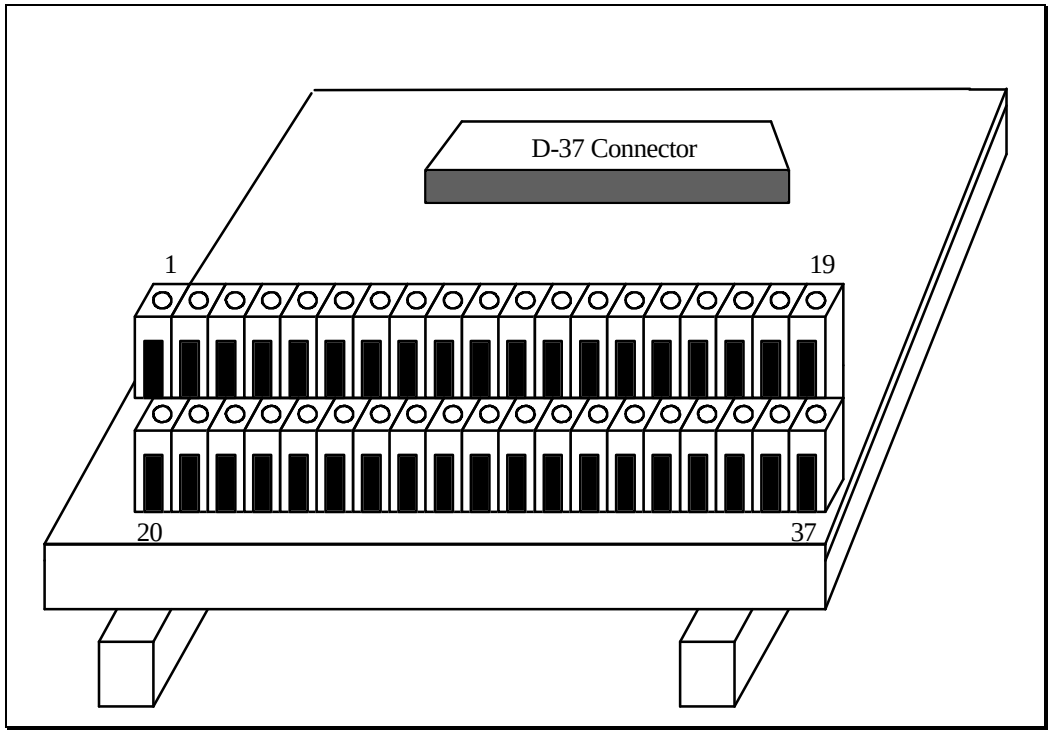

Figure 9. Terminal Block Box Illustration

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10. SPECIFICATIONS

A/D Converter	**12-Bit Version**	**16-Bit Version**
Acquisition + Conversion	2 µs + 8 µs	2 µs + 8 µs
Monotonicity	No missing codes	No missing codes
Integral linearity error	± 1 LSB	± 3 LSB
Differential linearity error	± 1 LSB	+3/-2 LSB
Full scale error	± 0.5 %	± 0.5 %
Aperture delay	40 ns	40 ns

Analog Input	
Number of input channels	8 differential / 16 single-ended, expandable to 256
Input range	±10, ±5, ±2.5, ±1.25V
Programmable gain	1, 2, 4, 8
Maximum over-voltage	±30 V
Input impedance	100 MΩ (DC)

A/D Miscellaneous Specifications	
Data FIFO depth	512 (standard) or 2048 (with 2K option) samples
Scan list length	512 (standard) or 2048 (with 2K option) entries
Scan speed	10 µs, 20 µs, 40 µs
Trigger source	Internal (Software) / External (TTL)
Trigger mode	Continuous / One-shot
External (TTL) trigger	0.8 V (low) / 2.2 V (high), Rising / Falling edges Latency to A/D scan < 1µs
Sampling rate	0.006 Hz to 100 kHz (with internal clock source)
External clock rate	DC - 5 MHz

Digital I/O	
Digital input channels	4 (no latch)
Digital output channels	4 (latched)
Maximum source current	0.5 mA
Maximum sinking current	2.5 mA
Minimum logic ‘1’ level	2.4 V
Maximum logic ‘0’ level	0.8 V

General Specifications	
Power consumption	160 mA (full power), 40 mA (power down)
Operating temperature	0 °C to 50 °C
Storage temperature	0 °C to 70 °C
Humidity	0 to 95%, non-condensing
Size (cable not included)	Standard PCMCIA type II
Weight	1.5 oz (for reference only)

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